one example, second capping layer 310 comprises Si_xN_y, Si_xC_y, SiC_xH_y, $SiC_xO_yN_z$ or SiC_xN_y. In one example, second capping layer 310 is about 150 Å to about 700 Å thick. Second capping layer 310 may be formed by high density plasma (HDP) or plasma enhanced CVD (PECVD) deposition. In a first example, second capping layer 310 is formed at a temperature of about 400°C. In a second example, second capping layer 310 is formed at a temperature of between about 350°C and about 450°C. Second capping layer 310 is thick enough either alone or in combination with first capping layer 300 to act as a copper diffusion barrier. Second capping layer 310 also acts, either alone or in combination with first capping layer 300, as an RIE stop layer for subsequently deposited ILD layer etching.

[Para 39] In FIG. 3I, an ILD layer 320 has been formed on a top surface 325 of second capping layer 315. An optional cryogenic clean may be performed immediately prior to formation of second capping layer 315. The steps illustrated in FIGs. 3A through 3I may be repeated as many times as required.

[Para 40] FIGs. 4A and 4B are partial cross-sectional views of a method of fabricating copper interconnect wires according to a second embodiment of the present invention. In FIG. 4A, first capping layer 300A comprises a lower first capping layer 330 and an upper first capping layer 335. In one example, lower first capping layer 330 and upper first capping layer 335 each independently comprise Si_xN_y, Si_xC_y, SiC_xH_y,

$SiC_xO_yN_z$ or SiC_xN_y. In one example, lower first capping layer 330 and upper first capping layer 335 are independently about 25 Å to about 100 Å thick. All capping layers of the present invention may comprise multiple layers as discussed *infra*.

[Para 41] In a first example, the total thickness (the thickness of lower first capping layer 330 plus the thickness of upper first capping layer 335) of first capping layer 300A is selected to be thin enough to allow optical microscopy and scanning electron microscopy (SEM) defect inspection and image size measurements of dual structures under the capping layer. In a second example, first capping layer 300A is thin enough to allow penetration of the capping layer by a probe tip during inline testing or parametric characterization. In all examples, first capping layer 300A is thick enough to prevent formation of $Cu_xO_yF_z$ particles or other Cu oxides or fluoride particles under the first capping layer. First capping layer 300A may not be thick enough to act as a copper diffusion barrier.

[Para 42] In FIG. 4B, second capping layer 310 is formed on top surface 340 of upper first capping layer 335. Again, a cryogenic cleaning process may be performed immediately prior to formation of second capping layer 310.

[Para 43] In a third embodiment of the present invention first capping layer 300 and second capping layer 310 each independently comprise two or more layers of materials

selected from the group consisting of Si_xN_y, Si_xC_y, SiC_xH_y, $SiC_xO_yN_z$ and SiC_xN_y, each layer of first capping layer 300 being, for example, between about 25 Å to about 100 Å thick and each layer of second capping layer 305 being, for example, between about 150 Å to about 700 Å thick.

[Para 44] FIG. 5 is a flowchart of the method of fabricating copper interconnect wires according to the present invention. The method may be practiced as described *supra* or may incorporate controlled storage and rework cleans as described *infra*.

[Para 45] In step 400, a substrate is provided with an ILD layer over a copper diffusion barrier layer as describe *supra* in reference to FIG. 3A. In one example, the substrate is a 200 mm or 300 mm bulk silicon or silicon-on insulator (SOI) semiconductor wafer. In step 405, wire trenches (and optionally via opening in the bottom of selected wire trenches and through the diffusion barrier layer) are formed in the ILD layer. The method can proceed three ways. The method can proceed directly to step 410 to step 415 or to step 420.

[Para 46] In step 410, a single or multiple layer liner is formed in the wire trenches (and in the via openings), a copper core conductor is formed and a CMP performed to form damascene (or dual damascene) wires in the ILD layer. The CMP may comprise a copper CMP step and a liner CMP step.

The method can proceed three ways. The method can proceed directly to step 410 to step 415 or to step 420.

[Para 47] In step 415, the substrate is stored in a controlled environment until the substrate can proceed to step 410. A controlled environment may comprise a humidity-controlled environment, an inert gas environment, a temperature controlled environment or combinations thereof. An example of a humidity-controlled environment is one in which the relative humidity is less than about 20%. An example of a temperature controlled environment one in which the temperature is maintained between about 60 °F and about 80 °F. An example of an inert atmosphere is one comprising H_2, He, Ar, N_2 and combinations thereof. Another example of an inert atmosphere is air with a relative humidity of about 20% or less

[Para 48] In step 420, if a copper surface has been exposed for an amount of time greater than a predetermined period of time, then a rework cleaning step is performed. In one example, the rework cleaning step is a dip in a 100:1 (by volume) aqueous dilute HF solution. In one example, it has been experimentally determined that the predetermined amount of time is about 17 hours at about 50% relative humidity and about 70°F. Then the method proceeds to step 410.

[Para 49] Returning to step 410, from step 410, the method can proceed three ways. The method can proceed to directly to step 425, to step 430 or to step 435.

[Para 50] In step 425, and optional cleaning step, which may be a reduction process (as opposed to an oxidation process) is performed and a first capping layer is formed over the damascene (or dual damascene) wires in the FSG layer as illustrated in FIG. 3F or 4A and described *supra*. The first capping layer is thin enough to allow inline optical or SEM inspection and measurements as well as inline electrical probing (testing). The first capping layer is thick enough to prevent formation of $Cu_XO_YF_Z$ particles. The first capping layer may not be thick enough to act as a copper diffusion barrier. The method then proceeds to step 440.

[Para 51] In step 440, inline inspection, measurement, testing and/or electrical probing is performed.

[Para 52] In step 435, if an amount of time greater than a predetermined period of time has elapsed, then a rework cleaning step is performed as described *supra* for step 420. Alternatively a rework liner CMP process (similar to the liner CMP step of step 410) may be performed which will polish off any Cu containing particles is performed. Then the method proceeds to step 440.

[Para 53] Returning to step 440, the method can proceed to step 445 or step 450. The method proceeds to step 445 only if a predetermined time limit has been exceeded and no first capping layer has been formed (step 425 was not performed) otherwise the method proceeds to step 450.

[Para 54] In step 450, an optional clean (which may be a cryogenic cleaning as described *supra*) is performed and the method proceeds to step 455.

[Para 55] In step 445, if an amount of time greater than a predetermined period of time has elapsed, then a rework cleaning step is performed as described *supra* for step 420. Alternatively a rework liner CMP process (similar to the liner CMP step of step 410) for the same or shorter amount of time may be performed which will polish off any Cu containing particles is performed. Then the method proceeds to step 455.

[Para 56] In step 455, either a second capping is formed on top of the first capping layer as illustrated in FIGs. 3H and 4B as described *supra*, or just a second capping layer is formed, or a single thicker version (same materials as described *supra*) of either the first or second capping layers is formed. The second capping layer is thick enough either alone or in combination with the first capping layer to act as a copper diffusion barrier. As discussed *supra*, each capping layer may comprise multiple layers, each layer comprising an

independently selected material formed by an independently selected process.

[Para 57] In step 460, further steps in the fabrication of an integrated circuit are performed, including one or more repetitions of steps 405 through 455 on additional wiring levels.

[Para 58] The present invention provides a method of fabricating copper interconnect wiring that reduces the risk of problems related to exposed copper surface reactivity and copper containing particle formation and thus provides a method of fabricating copper interconnect wiring that reduces the risk of problems related to the diffusion of copper while still providing a cost effective manufacturable process.

[Para 59] The description of the embodiments of the present invention is given above for the understanding of the present invention. It will be understood that the invention is not limited to the particular embodiments described herein, but is capable of various modifications, rearrangements and substitutions as will now become apparent to those skilled in the art without departing from the scope of the invention. For example, while the present invention has been described in the context of copper containing wires reacting with FSG glass to form $Cu_xO_yF_z$ particles, the present invention may be applied to preventing reactions of copper containing wires reacting with any dielectric material that forms unwanted particles such as

CuF, CuO, Cu_2O, Cu_2S, CuS or other copper containing particles. Therefore, it is intended that the following claims cover all such modifications and changes as fall within the true spirit and scope of the invention.